



Industrial Distinguished Lecturer Program by IEEE CAS Society (CASS) SBC60981AG



Date: 15.10.2024

Time : 02.30 PM to 04.00PM (UTC+05.30 Chennai)

Gmeet Link: <https://meet.google.com/kbj-kzxk-jpo>

Industrial Distinguished Lecturer: Prof. Sudipto Chakraborty

Title: Cryogenic CMOS design techniques for scaled quantum computing systems

On 15th October, we organized the Industrial Distinguished Lecturer Program through online mode. It started with the Welcome Address and Introduction of the Resource Person by the student Members Ms.Vivitha and Mr.Ramakrishnan, IEEE Circuits and Systems Society, Sri Sairam Engineering College. Next, the session was taken over by Prof. Sudipto. 40 participants attended this iDLP.



Professor explained that the Cryogenic CMOS (Complementary Metal-Oxide-Semiconductor) design techniques are critical for developing scalable quantum computing systems. These designs operate at cryogenic temperatures (close to absolute zero) to ensure compatibility with quantum devices like qubits, which require low thermal noise environments for stable operation. Cryogenic CMOS technology helps minimise power consumption and improve device performance at low temperatures. Key challenges include addressing the performance degradation of MOSFETs at cryogenic conditions and developing low-power circuits for qubit

control and readout. Optimizing interconnects and packaging techniques is essential to ensure seamless integration of quantum processors with classical control systems. Emerging techniques, such as leveraging subthreshold operation and novel transistor designs, aim to overcome these challenges and enable large-scale quantum computing systems.

INDUSTRIAL DISTINGUISHED LECTURER PROGRAM
15.10.24

SAI RAM ENGINEERING COLLEGE
West Tambaram, Chennai - 44

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PROF. SUDIPTO CHAKRABORTY
INDUSTRIAL DISTINGUISHED LECTURER PROGRAM

CRYOGENIC CMOS DESIGN TECHNIQUES FOR SCALED QUANTUM COMPUTING SYSTEMS

15 OCTOBER 2024 02.40 PM - 4.00 PM

LOCATION: VRR HALL

Ms.S.USHA
ADVISOR
SEC IEEE-CAS SBC

Dr.S.BRINDHA
PROFESSOR/ECE
SEC IEEE SB COUNSELLOR

Dr.J.THAMIL SELVI
HOD-ECE

Dr.J.RAJA
PRINCIPAL

Dr.Sai PRAKASH LEOMUTHU
CHAIRMAN & CEO
SAIRAM INSTITUTIONS

He also answered the queries asked by our students. The vote of thanks was proposed by Ms. Saigeetha is a student member of Sri Sai Ram Engineering College.

We take this opportunity to thank our **CEO, Principal, and HOD-ECE** for their support and guidance in successfully completing this Industrial Distinguished Lecturer Program.

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Sudipto Chakraborty (Presenting)

Future system block diagram comparison

Room temperature control

- All signals routed out of cryostat
- ~5n wires from RT to base, $n \ll$ # of qubits
- Connectors degrade reliability, increase cost
- Easier to cool RT electronics
- High fidelity RT electronics are easier

Cryogenic control

In near term, systems will not have the logical controller and syndrome matching

- Fewer signals routed out of cryostat
- ~5n wires only from 4K to base, $n \ll$ # of qubits
- Fewer connectors, more reliable, cheaper
- Harder to cool LT electronics
- High fidelity low-power LT electronics are difficult

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CAS AMERICAN CRYOGENIC SOCIETY IEEE

16:13 | IDLP on Cryogenic CMOS Design Techniques

Sudipto Chakraborty

Ramakrishnan Sriram

VIVITHA M G 2022-2026

SUBALAKSHMI L M

S.Nivedita

SAIGEETHA U

MONIKHA K 2022-2026

29 others

Usha S

Number of Participants: IEEE Members:25
 Non-IEEE Member:15
 CASS Members:15