



Industrial Distinguished Lecturer Program by IEEE CAS Society (CASS) SBC60981AG



Date: 12.02.25

Time: 10.30AM

Venue : Smart Class Room I

Industrial Distinguished Lecturer: **Mr.Boon Chong Ang,**
Application Engineer,
Intel, Malaysia.

Title: “Chiplet Design Overview: The Limit of Moore’s Law and Challenges in Chiplets”

On 12th February 2025 at 10.30am, the Department of ECE, Sri Sairam Engineering College, in association with **IEEE Circuits and Systems Society Student Branch Chapter** organized the Industrial Distinguished Lecturer Program. It started with the Welcome Address and Introduction of the Resource Person by **Prof. S, Usha, Advisor, IEEE Circuits and Systems Society, Sri Sairam Engineering College.** Next, Mr.Boon Chong Ang took over the session. Nearly 100 participants attended this IDLP.

The poster is for an event titled "INDUSTRIAL DISTINGUISHED LECTURE PROGRAM on CHIPLET DESIGN OVERVIEW". It features a green background with a central image of a chiplet. The text includes the date and time "12.02.2025, Wednesday | 10:30 AM" and the venue "Smart Class Room I". The resource person is "Mr. BOON CHONG ANG, Application Engineer, Intel, Malaysia". The poster also lists the organizing bodies: Sairam Institutions, IEEE Sairam, and the Department of Electronics and Communication Engineering at Sri Sairam Engineering College. Logos for various accreditation bodies like RAISE, EOMS, SDG, and others are at the bottom.

Sairam INSTITUTIONS **IEEE Sairam** SEC202502IEEECAS01

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING **CAS**

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Cordially Invite you for
INDUSTRIAL DISTINGUISHED LECTURE PROGRAM on
CHIPLET DESIGN OVERVIEW

12.02.2025, Wednesday | 10:30 AM
Smart Class Room I

Resource Person
Mr. BOON CHONG ANG
Application Engineer,
Intel, Malaysia

Mr. K. Srinivasan
Event Coordinator

Ms. S. Usha
Advisor
IEEE CAS

Dr. S. Brindha
IEEE SBC
Counsellor

Dr. J. Thamilselvi
HOD - ECE

Dr. J. Raja
Principal

Dr. Sai Prakash LeoMuthu
Chairman & CEO
Sairam Institutions

RAISE **EOMS** **SDG** **ARISA** **NIIF** **GOALS**

Professor explained that Chiplet design is an emerging solution to address the limitations of Moore's Law, which has seen slowing progress in transistor miniaturization. Moore's Law historically predicted that the number of transistors on a chip would double every two years, but physical and economic constraints are now limiting further gains. Chiplets allow for the modular integration of smaller, specialized components (chiplets) into a single package, enabling improved performance and scalability without the need for a monolithic design. This approach optimizes yield, reduces costs, and enhances flexibility. However, challenges in chiplet design include ensuring interoperability, managing complex packaging technologies, and dealing with the thermal and power constraints of integrating multiple chiplets. Additionally, designing a robust interconnect network between chiplets to ensure high-speed communication is a critical hurdle. Despite these challenges, chiplet-based architectures offer a promising path forward for continued innovation in semiconductor design. As the industry moves beyond Moore's Law, chiplets could play a key role in enabling the next generation of high-performance computing.



He also answered the queries asked by our students. The vote of thanks was proposed by Mr. K.Srinivasan, Professor from Sri Sai Ram Engineering College.

We take this opportunity to thank our **CEO sir, Principal sir, and HOD-ECE** for their support and guidance towards the successful completion of this Industrial Distinguished Lecturer Program.

Number of Participants: IEEE Members:70

Non-IEEE Member:30

CASS Members:40