SRI SAIRAM ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SAMPLE QUESTIONS FOR TEACHING LEARNING PROCESS

Domain: **INTEGRATED CIRCUITS**

1) CMRR of a differential amplifier can be improved by decreasing _____.

a. Differential voltage gain

b. Common mode voltage gain

c. Both a and b

d. None of the above

2) Which concept states that if one input terminal of an op-amp is at zero potential, then the other one also will be at zero potential?

a. Virtual short

b. Virtual ground

c. Zero input current

d. None of the above

3) Which among the following is/are included in DC characteristics of op-amp?

a. Input bias current

b. Thermal drift

c. Both a and b

d. None of the above

4) PSSR is an op-amp parameter which defines the degree of dependence on variations in _____.

a. temperature

b. pressure

c. power supply voltage

d. slew rate

5) What is PSRR value of an ideal op-amp?

a. Zero

b. Unity

c. Infinite

d. Unpredictable

6) Flicker noise is also regarded as _____.

a. Popcorn noise

b. 1/f noise

c. Both a and b

d. None of the above

7) Popcorn noise is generated by abrupt variations in input bias current especially due to imperfect surface conditions of _____.

a. Conductor

b. Insulator

c. Semiconductor

d. None of the above

8) Which among the following has a constant power spectral density over a wide frequency range?

a. White noise

b. Black noise

c. Pink noise

d. Blue noise

9) Which among the following is/are responsible for electrical interactions?

a. Parasitic capacitance

b. Mutual inductance

c. Both a and b

d. None of the above

10) The noise produced by the differential input stage can be reduced by the selection of

a. Proper transistor type

b. Proper geometry

c. Adequate level of operating currents

d. All of the above

11) In an inverting ideal integrator, which component exhibits the feedback path connection?

a. Resistor

b. Inductor

c. Capacitor

d. Diode

12) In absence of any applied AC input signal, what would be the gain of an ideal integrator?

a. Zero

b. Unity

c. Infinity

d. Unpredictable

13) As the frequency increases, input impedance of differentiator _____.

a. Increases

b. Decreases

c. Remains constant

d. None of the above

14) In a buffer circuit, the voltage follower is placed _____ two networks in order to minimize the effect of loading on the first network.

a. Before

b. Between

c. After

d. None of the above

15) Due to presence of a capacitor in feedback path, the output of an integrator varies

a. Gradually

b. Instantaneously

c. Intermittently

d. All of the above

16) Which among the following circuits is also regarded/known as ' Threshold Detector '?

a. Window detector

b. Over voltage indicator

c. Level detector

d. Zero crossing detector

17) In an inverting Schmitt Trigger circuit, the hysteresis _____ is also known as 'hysteresis width'.

a. voltage

b. current

c. resistance

d. power

18) In hysteresis width, the hysteresis voltage is equal to _____ upper & lower threshold voltages (V_{UT} & V_{LT}).

a. sum of

b. difference between

c. product of

d. division of

19) In a peak detector circuit, which component holds the peak value till a higher peak value is detected?

a. Diode

b. Inductor

c. Capacitor

d. MOSFET switch

20) Among which of the following factors do/does the operation of sample and hold mode depend/s?

a. Input

b. Output

c. Position of switch

d. All of the above

21) In DACs, gain error occurs due to _____.

a. offset voltages of op-amps

b. leakage current in the switches

c. error in feedback resistor value

d. error in current source resistance values

22) Which among the following types of ADCs require/s the shortest conversion time?

a. Flash type

b. Successive Approximation

c. Dual Slope

d. All of the above

23) In dual slope type of ADCs, an input hold time is _____.

a. Almost zero

b. Higher than that of flash type ADCs

c. Longest

d. All of the above

24) In ADCs, it is possible to reduce the quantization error by _____the number of bits.

a. Increasing

b. Decreasing

c. Maintaining consistency in

d. All of the above

25) In ADC 0809 acting as a CMOS device, how many analog inputs & channel multiplexers are present?

a. 2

b. 4

c. 8

d. 16

26) Which characteristic of PLL is defined as the range of frequencies over which PLL can acquire lock with the input signal?

a. Free-running state

b. Pull-in time

c. Lock-in range

d. Capture range

27) According to transfer characteristics of PLL, the phase error between VCO output & incoming signal must be maintained between _____ in order to maintain a lock.

a. 0 & π

b. 0 & $\pi/2$

c. 0 & 2π

d. π & 2π

28) In VCO IC 566, the value of charging & discharging is dependent on the voltage applied at _____.

a. Triangular wave output

b. Square wave output

c. Modulating input

d. All of the above

29) For a PLL IC 565 with timing resistor & timing capacitor of about 15 kΩ & 0.02μF respectively, what would be the value of output frequency (f0)?

a. 433.33 Hz

b. 833.33 Hz

c. 1000 Hz

d. 2500 Hz

30) In AM detector using PLL, the phase detector is basically a multiplier which produces _____components of frequencies at its output.

a. Sum

b. Difference

c. Both a and b

d. None of the above

31) What is PSRR value of an ideal op-amp?

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b. Unity

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35) CMRR of a differential amplifier can be improved by decreasing _____.

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36) In a linear IC voltage regulator, series pass transistor always operates in _____ region.

a. Active

b. Saturation

c. Cut-off

d. All of the above

37) Switching regulators are series type regulators, which has _____ power dissipation & _____ efficiency.

a. increased, increased

b. increased, reduced

c. reduced, increased

d. reduced, reduced

38) The % load regulation of a power supply should be ideally _____ & practically _____.

a. zero, small

b. small, zero

c. zero, large

d. large, zero

39) Which performance parameter of a regulator is defined as the change in regulated load voltage due to variation in line voltage in a specified range at a constant load current?

a. Load regulation

b. Line regulation

c. Temperature stability factor

d. Ripple rejection

40) Which among the following factors affect/s the output voltage of a regulated power supply?

a. Load current

b. Input voltage

c. Temperature

d. All of the above

41) In PLL, the capture range is always _____the lock range.

a. Greater than

b. Equal to

c. Less than

d. None of the above

42) Once the phase is locked, the PLL tracks the variation in the input frequency. This indicates that _____

a. Output frequency changes by same amount as that of input frequency

b. Output frequency does not change as that of input frequency

c. There is no relation between input & output frequencies

d. None of the above

43) In the locked state of PLL, the phase error between the input & output is _____.

a. Maximum

b. Moderate

c. Minimum

d. All of the above

44) In communication circuits, PLL is currently applicable for _____

a. Demodulation applications

b. Tracking a carrier or synchronizing signal

c. Both a and b

d. None of the above

45) Basically, PLL is used to lock _____

a. Its output frequency

b. Phase to the frequency

c. Phase of the input signal

d. All of the above

46) Offset error is basically defined as the non-zero level of analog output especially when all the digital inputs are ____.

a. 0

b. 1

c. Both a and b

d. None of the above

47) In DACs, which type of error/s specify/ies the amount by which the actual output of DAC differ from ideal straight line transfer characteristics?

a. Linearity error

b. Offset error

c. Gain error

d. All of the above

48) Which among the following characteristics of D/A converter occur/s due to resistor and semiconductor aging?

a. Speed

b. Settling time

c. Long term drift

d. Supply rejection

49) In DAC, resolution increases with the _____ in number of bits.

a. Increase

b. Decrease

c. Constant

d. None of the above

50) In weighted resistor DAC, how many resistors per bit is/are required?

a. One

b. Two

c. Three

d. Four