SRI SAIRAM ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SAMPLE QUESTIONS FOR TEACHING LEARNING PROCESS

Domain: **DIGITAL ELECTRONICS**

1) Match the following value kind attributes with their return elements:

A. Value Type attribute -------------------- 1) Length

B. Value Array attribute ------------------- 2) Information

C. Value Block attribute ------------------- 3) Bounds

a. A- 3, B- 1, C- 2

b. A- 1, B- 2, C- 3

c. A- 2, B- 1, C- 3

d. A- 2, B- 3, C-1

2) Which among the following is not a type of concurrent statement?

a. Simple signal assignment

b. Selected signal assignment

c. Generate statement

d. Direct Instantiation

3) Which type of logic is produced by case statements?

a. Serial logic

b. Parallel logic

c. Priority encoded logic

d. Priority decoded logic

4) Which among the following does not belong to the category of sequential statements?

a. If statements

b. Process statements

c. Loop statements

d. Node statements

5) What does an arrow indicate in the schematic format of process statement given below?

Process Statement Representation.png

a. Variable declaration

b. Process body

c. Process label

d. Sensitivity list

6) Which among the following ROMs exhibit/s the necessity of eliminating the PROM from the circuit?

a. EPROM

b. EEPROM

c. Both a and b

d. None of the above

7) Which signal is used to transfer the stored data into RAM?

a. Store

b. Load

c. Recall

d. Move

8) Which components play a significant role in the formation of a dynamic RAM?

a. Two MOSFETs

b. Two capacitors

c. One MOSFET and one capacitor

d. One MOSFET and two capacitors

9) What is the bit storage capacity of TTL RAM cell?

a. 0

13) In the below drawn schematic, what does an arrow between the circles indicate?
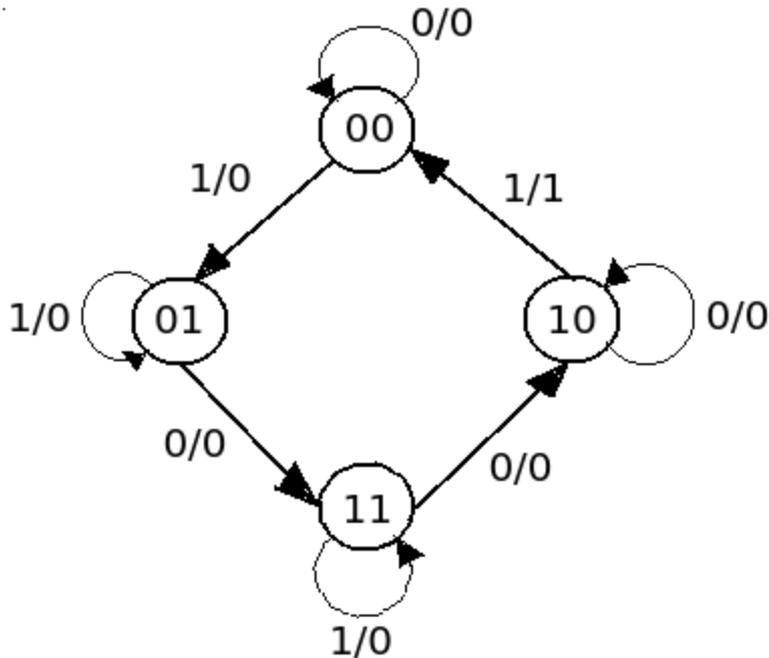
a. Present state

b. Next state

c. State transition

d. Don't care condition

14) From the K-map given below, what would be the state equation of D Flip Flop?
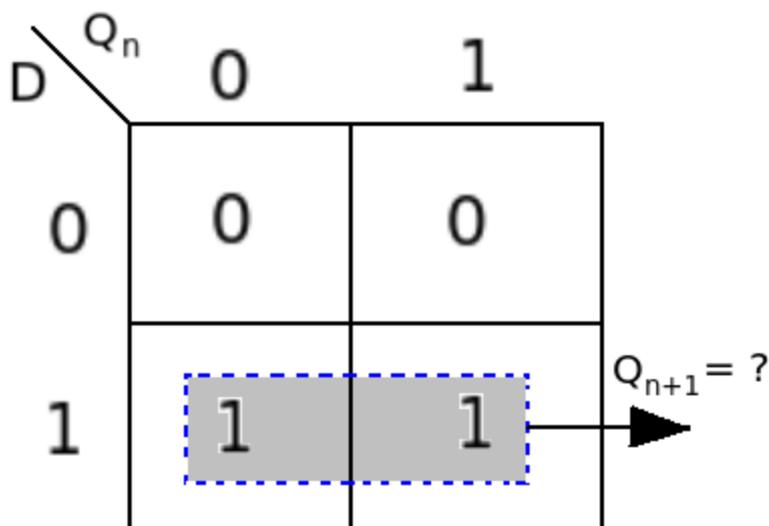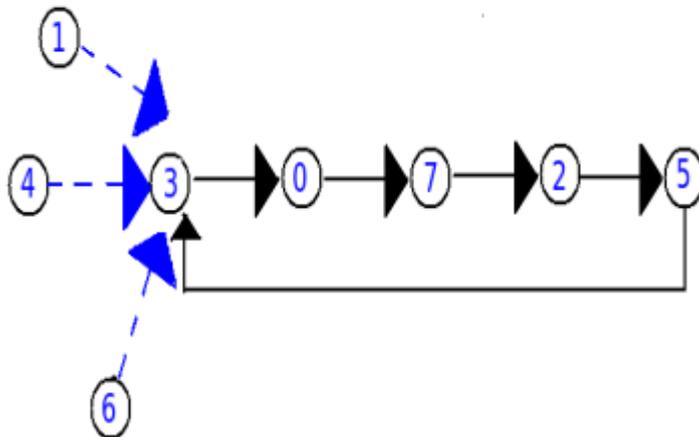
a. Qn+1 = QnD

b. Qn+1 = QnD

c. Qn+1 = D

d. Qn+1 = D

15) The mechanism of 'Bushing' specifically refers to the addition of _____ in the state diagram

a. Nodes

b. Branches

c. Loops

d. States

16) How many 'D' flip flops will be required for designing the synchronous counter for the state diagram shown below?

a. 2

b. 3

c. 5

d. 7

17) Which among the following are the sequential circuits entering into the phenomenon of lock out condition?

a. Bush circuits

b. Bushless circuits

c. Locked circuits

d. Unlocked circuits

18) From the diagram shown below, if the circuit enters into state '5', its next state will be '7'. If the circuit further enters at state '7', then what would be the desirable next state for avoiding the lock out condition?
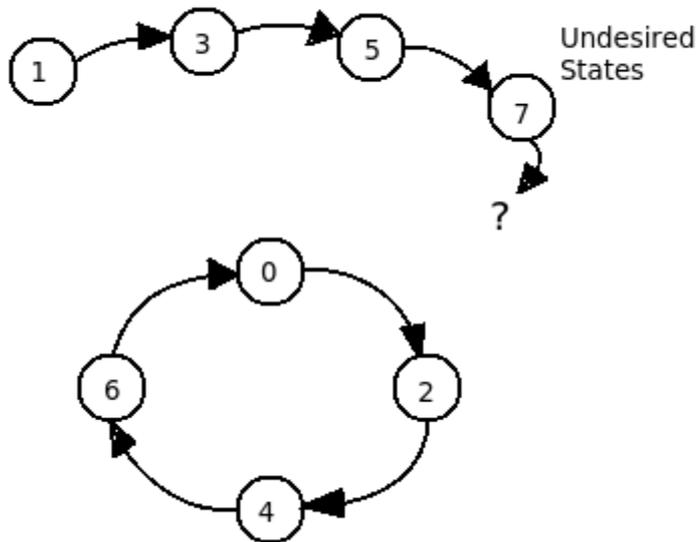
a. 0

b. 3

c. 5

d. 7

19) Which among the following sequential logic circuits are adopted for the designing of a sequence generator?

a. Shift Registers

b. Counters

c. Both a and b

d. None of the above

20) In a sequence detector, if the required bit is at its input while checking the sequence bit by bit, the detector moves to _____

a. Previous state

b. Next state

c. Remains in the same state (present state)

d. Null state

21) Which among the following is not a mode of Flip Flop representation?

a. Characteristic Equations

b. Excitation Tables

c. Finite State Machines (FSM)

d. Variable Entered Mapping (VEM)
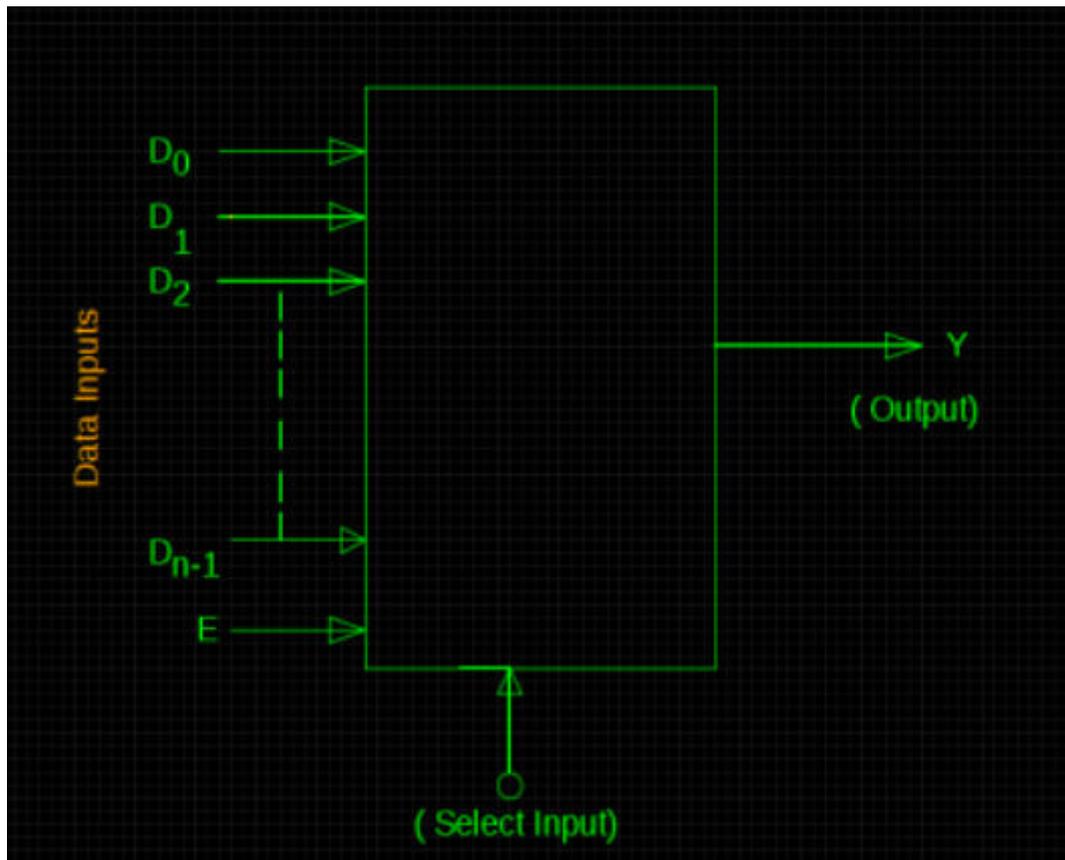
22) Which flip-flop plays a vital role by functioning as the basic building block of a ripple counter?

a. S-R flip-flop

b. J-K flip-flop

c. D flip-flop

d. T flip-flop

23) Which among the following is an octal to binary priority encoder?

a. 74147

b. 74148

c. 74149

d. 74150

24) Which type of combinational logic circuit is shown below?

a. Multiplexer

b. Demultiplexer

c. Encoder

d. Comparator

25) Which is the simplified equation of output for K-map consisting of four adjacent ones, given below?
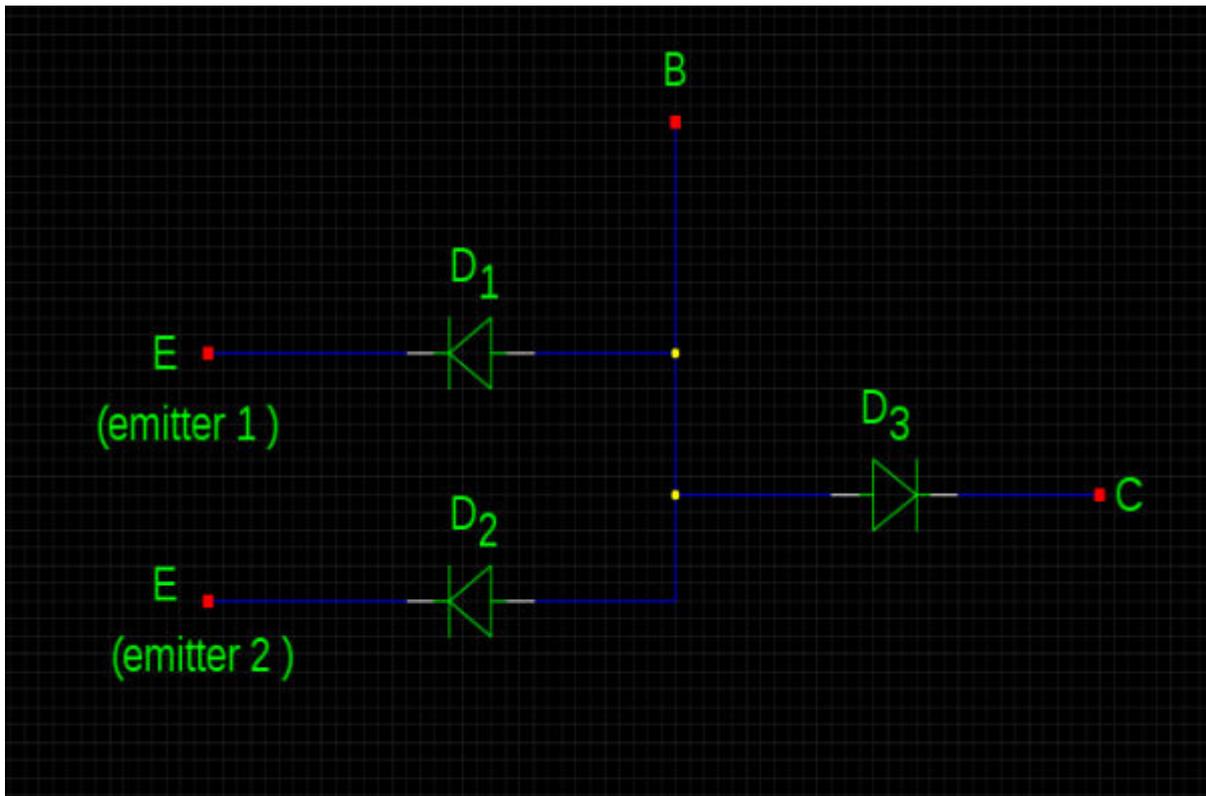
a. A B

b. BD

c. CD

d. ABD

26) Which is the correct order of sequence for representing the input values in K-map?

a. (00, 01, 10, 11)

b. (00, 10, 01, 11)

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c. (00, 01, 11, 10)

d. (00, 10, 11, 01)

27)   What does the diode D3 represents in the equivalent circuit of Multiple Emitter Transistor shown below?

a. Base to emitter junction

b. Collector to base junction

c. Collector to emitter junction

d. Emitter to emitter junction

28)   If power dissipation and propagation delay in a logic circuit are estimated to be 55mW and 20ns respectively, what will be its figure of merit?

a. 1.10 nanojoule

b. 1.65 nanojoule

c. 2.50 nanojoule

d. 5.5 nanojoule

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29) How are the design specifications represented in the behavioral modeling style of VHDL?

a. Boolean equation

b. Truth table

c. Logical diagram

d. State diagram

30) Dataflow style of architectural modeling is represented as a set of _____ assignment statements.

a. Sequential

b. Concurrent

c. Random

d. Combinational

31) Which type of architectural modeling style describes the internal design details in the form of a set representing the interconnected components?

a. Dataflow

b. Behavioral

c. Structural

d. Mixed

32) Which among the following is the correct way of entity representation for the two input NAND gate shown below?

a. NAND 5 entity is

port (A, B : input;

C: output);

NAND 5 end;

b. entity NAND5 is

port (A, B : in bit;

C: out bit);

end NAND 5;

c. Entity: NAND5

port(Inputs: A, B;

Output : C);

end;

d. entity : NAND5

port(inbit : A,B),

(outbit: C);

end.

33) Which parameter of read cycle timing characteristics defines the maximum time delay between the beginning of read pulse and output buffers arriving at active state from Hi-z condition?

a. Read to output valid time

b. Read to output active time

c. Access time

d. Output tristate from read time

34) Which among the following specifies the minimum amount of time necessary for data validation after the termination of the write pulse?

a. Write pulse time

b. Write release time

c. Data set up time

d. Data hold up time

35) Which among the following techniques is used by EPROM for erasing purpose?

a. Force Convection

b. Ultraviolet Radiation

c. Photo-conduction

d. None of the above

36) Which operations are likely to get performed by the Content Accessible Memories (CAM) in addition to read/write operations executed by conventional memories?

a. Association

b. Distribution

c. Commutation

d. Identification

37) In JTAG programming, JTAG stands for _____

a. Joint Texture Analysis Group

b. Joint Technique Aided Group

c. Joint Testing Array Group

d. Joint Test Action Group

38) What would happen, if smaller logic modules are utilized for performing logical functions associated with FPGA?

A. Propagation delay will increase

B. FPGA area will increase

C. Wastage of logic modules will not be prevented

D. Number of interconnected paths in device will decrease

a. A & B

b. C & D

c. A & D

d. B & C

39) What is/are the configurable functions of each and every IOBs connected around the FPGA device from the operational point of view?

a. Input operation

b. Tristate output operation

c. Bi-directional I/O pin access

d. All of the above

40) Which type of CPLD packaging can provide maximum number of pins on the package due to small size of the pins?

a. PLCC

b. QFP

c. PGA

d. BGA

41) Which mechanism allocates the binary value to the states in order to reduce the cost of the combinational circuits?

a. State Reduction

b. State Minimization

c. State Assignment

d. State Evaluation

42) Which among the following state machine notations are generated outside the sequential circuits?

a. Input variables

b. Output variables

c. State variables

d. Excitation variables

43) Consider the state equation given below. If R.H.S of an equation is zero, then what would be the value of L.H.S (next state) after the application of a clock pulse?

$QA(n + 1) = (QA\ QB\ +\ QA\ QB)\ x + QA\ QB$

a. Zero

b. Infinity

c. QA QB x

d. QA QB x

44) Where are signals received from, at the output decoder in generalized form of Mealy circuit?

A. Input of memory elements

B. Output of memory elements

C. External inputs

D. External outputs

a. A & D

b. B & C

c. B & D

d. A & C

45) Why is the extent of propagation delay in synchronous counter much lesser than that of asynchronous counter?

a. Due to clocking of all flip flops at the same instant

b. Due to increase in number of states

c. Due to absence of connection between output of preceding flip flop and clock of next one

d. Due to absence of mode control operation

46) Which flip flops serve to be the fundamental building blocks of counters?

a. S-R flip flops

b. J-K flip flops

c. T flip flops

d. D flip flops

47) On which factor/s does the clock pulse frequency of a counter depend/s for its reliable operation?

a. Number of flip flops

b. Width of strobe pulse

c. Propagation delay

d. All of the above

48) If the output of two-bit asynchronous binary up counter using T flip flops is '00' at reset condition, then what output will be generated after the fourth negative clock edge?

a. 00

b. 01

c. 10

d. 11

49) If a complete sequence is detected, what will be the output of a sequence detector?
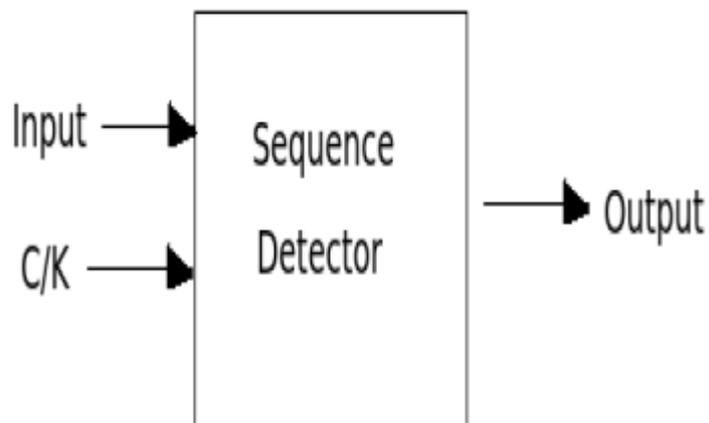
a. 1

b. 0

c. Both a and b

d. None of the above

50) On the second falling edge of clock in ring counter, if the generated output of second clock pulse is ' 0100', what will be the output after the fourth clock pulse?

a. 1000

b. 0001

c. 0010

d. 0000

ANSWER: 0001

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