SRI SAIRAM ENGINEERING COLLEGE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SAMPLE QUESTIONS FOR TEACHING LEARNING PROCESS

Domain: **MICROCONTROLLERS AND APPLICATIONS**

1) Which flags of status register are most likely to get affected by the single-cycle increment and decrement instructions?

a. P Flags

b. C Flags

c. OV Flags

d. Z Flags

2) Where is the result stored after an execution of increment and decrement operations over the special - purpose registers in PIC?

a. File Register

b. Working Register

c. Both a & b

d. None of the above

3) Which instruction is applicable to set any bit while performing bitwise operation settings?

a. bcf

b. bsf

c. Both a & b

d. None of the above

4) What does the 'program idata' section of data memory contain in C-18 Compiler?

a. statically assigned/allocated initialized user variables

b. statically assigned /allocated uninitialized user variables

c. only executable instructions

d. variables as well as constants

5) In which aspects do the output functions specified in stdio.h differ from ANSI specified versions?

a. Provision of MPLAB specific extensions

b. Floating-point Format Support

c. Data in Program Memory

d. All of the above

6) Which command-line option of compiler exhibits the banner comprising overall number of errors, messages, warnings and version number after an accomplishment of the compilation process?

a. help

b. verbose

c. overlay

d. char

7) Which among the below assertions represent the salient features of PIC in C-18 compiler?

a. Transparent read/ write access to an external memory

b. Provision of supporting an inline assembly during the necessity of an overall control

c. Integration with MPLAB IDE for source-level debugging

d. All of the above

8) Which register/s should set the SPEN bit in order to configure RC7/RX/DT pins as DT (data lines)?

a. TXSTA

b. RCSTA

c. Both a & b

d. None of the above

9) Which bit plays a salient role in defining the master or slave mode in TXSTA register especially in synchronous mode?

a. RSRC

b. CSRC

c. SPEN

d. SYNC

10) What is the status of shift clock supply in an USART synchronous mode?

a. Master-internally, Slave-externally

b. Master-externally, Slave-internally

c. Master & Slave (both) - internally

d. Master & Slave (both) - externally

11) How is the baud rate specified for high-speed (BRGH = 1) operation in an asynchronous mode?

a. FOSC / 8 (X + 1)

b. FOSC / 16 (X + 1)

c. FOSC / 32 (X + 1)

d. FOSC / 64 (X + 1)

12) Why is the flag bit TXIF tested or examined in the PIR1 register after shifting all the data bits during the initialization process of USART in asynchronous mode?

a. For ensuring the transmission of byte

b. For ensuring the reception of byte

c. For ensuring the on-chip baud rate generation

d. For ensuring the 9th bit as a parity

13) What is the purpose of a special function register SPBRG in USART?

a. To control the operation associated with baud rate generation

b. To control an oscillator frequency

c. To control or prevent the false bit transmission of 9th bit

d. All of the above

14) Where should the value of TX9 bit be loaded during the 9 bit transmission in an asynchronous mode?

a. TXSTA

b. RCSTA

c. SPBRG

d. All of the above

15) How many upper bits of SSPSR are comparable to the address located in SSPADD especially after the shifting of 8 bits into SSPSR under the execution of START condition?

a. 7

b. 8

c. 16

d. 32

16) Where does the baud rate generation occur and begins to count the bits required to get transmitted, after an execution (set) of BF flag?

a. SCL line

b. SDA line

c. Both a & b

d. None of the above

17) Which command/s should be essentially written for I2C input threshold selection and slew rate control operations?

a. SSPSTAT

b. SSPIF

c. ACKSTAT

d. All of the above

18) Which bits assist in determining the I2C bit rate during the initialization process of MSSP module in I2C mode?

a. SSPADD

b. SSPBUF

c. Both a & b

d. None of the above

19) What should be the value of SSPM3:SSPM0 bits so that SPI can enter the slave mode by enabling SS pin control?

a. 0000

b. 0100

c. 0010

d. 0001

20) Which bit of SSPCON must be necessarily set so as to enable the synchronization of serial port?

a. WCOL

b. SSPOV

c. CKP

d. SSPEN

21) Which among the below stated conditions are selected by the SSPCON & SSPSTAT control bits?

a. Slave Select mode in slave mode

b. Data input sample phase

c. Clock Rate in master mode

d. All of the above

22) Which among the below stated components should be filtered for determining the cut-off frequency corresponding to the PW period of low-pass filter?

a. Fundamental FPWM & higher harmonics

b. Resonant FPWM & higher harmonics

c. Slowly Varying DC components

d. Slowly Varying AC components

23) How do the variations in an average value get affected by PWM period?

a. Longer the PWM period, faster will be the variation in an average value

b. Shorter the PWM period, faster will be the variation in an average value

c. Shorter the PWM period, slower will be the variation in an average value

d. Longer the PWM period, slower will be the variation in an average value

24) What would be the resolution value if oscillator and PWM frequencies are 16MHz and 2 MHz respectively?

a. 2

b. 3

c. 4

d. 8

25) Why are the pulse width modulated outputs required in most of the applications?

a. To control average value of an input variables

b. To control average value of output variables

c. Both a & b

d. None of the above

26) Where does the comparison level occur for 16-bit contents in the compare mode operation?

a. Between CCPR1 register & TMR1

b. Between CCPR1 & CCPR2 registers

c. Between CCPR2 register & TMR1

d. Between CCPR2 register & TMR0

27) How does the pin RC2/CCP1 get configured while initializing the CCP module in the compare mode of operation?

a. As an input by writing it in TRISC register

b. As an output by writing it in TRISC register

c. As an input without the necessity of writing or specifying it in TRISC register

d. Compare mode does not support pin RC2/CCP1 configuration CCP initialization

28) What is the fundamental role exhibited by the CCP module in compare mode in addition to timer 1?

a. To vary the pin status in accordance to the precisely controlled time

b. To vary the duty cycle of the rectified output

c. To vary the oscillator frequencies in order to receive larger periods

d. To vary the status of synchronization levels

29) The capture operation in counter mode is feasible when mode of CCP module is _____

a. synchronized

b. asynchronized

c. synchronized as well as asynchronized

d. irrespective of synchronization

30) Which register is suitable for the corresponding count, if the measurement of pulse width is less than 65,535 μs along with the frequency of 4 MHz?

a. 4-bit register

b. 8-bit register

c. 16-bit register

d. 32-bit register

31) What happens when the program control enters the Interrupt Service Subroutine (ISS) due to enabling of CCP1IE bit in PIE1 especially during the initialization of CCP1 Module in capture mode?

a. CCP1F bit gets cleared in PIR1 by detecting new capture event

b. GIE bit gets enabled

c. Contents of CCPR1L & CCPR1H are automatically copied in TMR1L & TMR1H respectively

d. Interrupt flag bit CCP1IF gets enabled in PIR

32) What among the below specified functions is related to PWM mode?

a. Generation of an interrupt

b. Generation of rectangular wave with programmable duty cycle with an user assigned frequency

c. Variations in the status of an output pin

d. Detection of an exact point at which the change occurs in an input edge

33) Which mode allows to deliver the contents of 16-bit timer into a SFR on the basis of rising/falling edge detection?

a. Capture Mode

b. Compare Mode

c. PWM Mode

d. MSSP Mode

34) Which among the below mentioned aspect issues are supported by capture/compare/PWM modules corresponding to time in PIC 16F877?

a. Control

b. Measurement

c. Generation of pulse signal

d. All of the above

35) The functionalities associated with the pins RA0- RA3 in ADCON1 are manipulated by _____

a. PCFG1 & PCG0

b. VREF

c. ADON

d. All of the above

36) What would be the value of ADC clock source, if both the ADC clock bits are selected to be '1'?

a. FOSC/2

b. FOSC/8

c. FOSC/32

d. FRC

37) Which bit is mandatory to get initiated or set for executing the process of analog to digital conversion in ADCON0?

a. ADIF

b. ADON

c. Go/!Done

d. ADSC1

38) Which channel would be selected if the values of channel bits CHS0 & CHS1 are '1' & '0' respectively in ADC Status Register?

a. AIN0

b. AIN1

c. AIN2

d. AIN3

39) Which bits play a crucial role in specifying the details or reasons associated with the system wake-up in WDT?

a. PD & TO

b. C & Z

c. DC & RPO

d. All of the above

40) Which command enables the PIC to enter into the power down mode during the operation of watchdog timer (WDT)?

a. SLEEP

b. RESET

c. STATUS

d. CLR

41) How much delay is required to synchronize the external clock at TOCKI in Timer '0' of PIC 16C61?

a. 2-cycles

b. 4-cycles

c. 6-cycles

d. 8-cycles

42) How much time is required for conversion per channel if PIC 16C71 possesses four analog channels, each comprising of 8-bits?

a. 10 μs

b. 15 μs

c. 20 μs

d. 30 μs

43) Where do the conversion interrupt flag (ADIF) end after an accomplishment of analog-to-digital (ADC) conversion process?

a. INTCON

b. ADCON0

c. OPTION

d. None of the above

44) What is the purpose of setting TOIE bit in INTCON along with GIE bit?

a. For setting the TOIF flag in INTCON due to generation of Timer 0 overflow interrupt

b. For setting the TOIE flag in INTCON due to generation of Timer 0 overflow interrupt

c. For setting the RBIF flag in INTCON due to generation of PORTB change interrupt

d. None of the above

45) Consider the following statements. Which of them is /are incorrect?

A. By enabling INTE bit of an external interrupt can wake up the processor before entering into sleep mode.

B. INTF bit is set in INTCON only when a valid interrupt signal arrives at INT pin.

C. During the occurrence of interrupt, GIE bit is set in order to prevent any further interrupts.

D. goto instruction written in program memory cannot direct the program control to ISR.

a. A & B

b. C & D

c. Only A

d. Only C

46) Which bit-register pair plays a significant role in configuring the rising or falling edge triggering levels in external interrupts of PIC 16C61/71?

a. INTF bit - INTCON register

b. INTEDG bit - OPTION register

c. INT bit -INTCON register

d. INTE bit - OPTION register

47) What kind of external edge-sensitive interrupt is generated due to transition effect at pin RBO/INT?

a. INT

b. RBO

c. INTF

d. All of the above

48) Which condition results in setting the GIE bit of INTCON automatically?

a. Execution of retfie instruction at the beginning of ISR

b. Execution of retfie instruction at the end of ISR

c. Execution of retfie instruction along with interrupt enable bit

d. Execution of retfie instruction along with interrupt disable bit

49) Which among the below specified combination of interrupts belong to the category of the PIC 16C61 / 71?

a. External, Timer/Counter & serial Port Interrupts

b. Internal, External & Timer/Counter Interrupts

c. External, Timer 0 & Port B Interrupts

d. Internal, External, Timer 0 & PortA Interrupts

50) What is the purpose of acquiring two different bits from INTCON register for performing any interrupt operation in PIC 16C61 / 71?

a. One for enabling & one for disabling the interrupt

b. One for enabling the interrupt & one for its occurrence detection

c. One for setting or clearing the RBIE bit

d. None of the above